PATENT

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WASHINGTON, D.C. 20231

ATTENTION: BOX PATENT APPLICATION

Sir:

Transmitted herewith for filing is the patent application of

Inventor(s): **Aftab Ahmad**

For: **FABRICATION OF INTEGRATED DEVICES USING NITROGEN IMPLANTATION**

Enclosed are:

(X) This application is a divisional of prior application 08/871,210, filed June 9, 1997.

(X) Two (2) formal sheets of drawing.

(X) A copy of Declaration from prior application is enclosed.

(X) Incorporation by Reference. The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

(X) Return prepaid postcard.

(X) Preliminary Amendment is enclosed. Please enter the Preliminary Amendment, cancelling Claims 16 - 22, prior to calculating the filing fee as follows:

CLAIMS AS FILED

FOR	NUMBER FILED	NUMBER EXTRA	RATE	FEE
Basic Fee			$760	$760
Total Claims	21 - 20 =	1 ×	$18	$ 18
Independent Claims	4 - 3 =	1 ×	$78	$ 78
TOTAL FILING FEE				$856

(X) A check in the amount of $856.00 to cover the filing fee is enclosed.

(X) The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Account No. 11-1410. A duplicate copy of this sheet is enclosed.

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Washington, D.C. 20231

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Attorney Docket No.	:	MICRON.061DV1
Applicant(s)	:	Aftab Ahmad
For	:	FABRICATION OF INTEGRATED DEVICES USING NITROGEN IMPLANTATION
Attorney	:	Adeel S. Akhtar
"Express Mail" Mailing Label No.	:	EL452638046US
Date of Deposit	:	September 17, 1999

I hereby certify that the accompanying

Transmittal in Duplicate; Specification in 13 pages; Preliminary Amendment in 2 pages; 2 sheets of drawings; Copy of signed Declaration by Inventor; Check for Filing Fee; Return Prepaid Postcard

are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and are addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

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MICRON.061DV1 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Aftab Ahmad	) Group Art Unit Unknown
Appl. No.	:	Unknown	)
Filed	:	Herewith	)
For	:	FABRICATION OF INTEGRATED DEVICES USING NITROGEN IMPLANTATION	)
Examiner	:	Unknown	)

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to examination on the merits, please amend the above-captioned application as indicated below.

IN THE SPECIFICATION:

On page 1, after the title, please add the following heading and paragraph:

--Reference to Related Application

The present application is a divisional of U.S. Application Serial No. 08/871,210, filed June 9, 1997.--

IN THE CLAIMS:

Please cancel Claims 16-22.

Appl. No.	**:**	**Unknown**
Filed	**:**	**Herewith**

<u>CONCLUSIONS</u>

In view of the foregoing amendments, Applicant respectfully submits that the application is in condition for examination on the merits.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: September 16, 1999

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FABRICATION OF INTEGRATED DEVICES USING NITROGEN IMPLANTATION

Background of the Invention

Field of the Invention

The present invention generally relates to semiconductor integrated device design and fabrication and, more particularly, to techniques for improving hot carrier resistance in ULSI transistors, such as CMOSFETs in random access memories (RAMs).

Description of the Related Art

In the past ten years, the scale of integration of semiconductor devices has increased significantly. More and more devices, such as CMOS type devices, have been positioned on smaller and smaller sized silicon substrates. In this trend toward higher packing density, the channel lengths of insulated gate field effect transistors have been drastically decreased to fabricate the smaller devices needed for these higher scale integration integrated circuits. However, as the devices approach the sub-micron level for CMOS technology, the channel length of the CMOS devices are so small that functional problems result.

In particular, source/drain punchthrough and hot electron susceptibility are the most critical detrimental short channel effects in CMOS device structures. Source/drain punchthrough occurs when the depletion regions of both the source and the drain of a transistor meet in the channel therebetween and create a depleted region extending from the drain region to the source region. Hence, the inverted channel region, which is located under the gate oxide, is lost due to overlapping source and drain regions. This situation eliminates gate control over the transistor and causes significant current leakages, especially when the transistor is in the "off" state. Presently, this effect can be reduced by positioning antipunchthrough implants in the channel regions during the fabrication process, such as Boron for n-channel devices and Phosphorus or Arsenic for p-channel devices, that prevent the depletion regions from meeting.

The other important problem that results from the short channel structures resulting from sub-micron CMOS dimension is hot electron susceptibility which is defined as the injection of high energy electrons into the gate oxide layer and farther into the polysilicon forming the gate of the CMOS structure. This electron injection into the gate oxide is mainly caused by the high electric field occurring at the drain contact of the transistor and severely reduces the threshold voltage of the transistor. In general, hot electron injection can be reduced by oxidizing the gate edge next to the drain region. Thus, oxidation rounds the gate edge and increases the gate oxide thickness at the gate edges. However, in ULSI applications, the oxide is not a good dielectric for the higher electric fields in these applications.

Alternatively, lightly-doped drain (LDD) structures, which are uniquely designed drain structures, are also advantageously used to overcome the hot electron injection problem. Particularly, in an LDD structure, the source/drain regions are formed by implanting two different ions with different doping densities. As a result, a lightly doped drain region, which is adjacent the channel region, separates the channel region from a heavily doped drain region. This lightly doped region significantly reduces the high electric field which causes hot electron injection into the gate oxide. However, ever decreasing device dimensions have brought many constraints to conventional LDD process technologies.

Specifically, in CMOS ULSI applications, a proper LDD drain should provide adequate hot-carrier protection for the device. In fact, there are many approaches in CMOS technology to provide such optimum LDD structures to prevent hot-electron injection into the gate oxide. One important technique is nitrogen implantation into the source/drain regions during the manufacture of NMOSFETs and PMOSFETs prior to the sidewall-spacer (SiO_2) formation. After the sidewall SiO_2 spacer deposition, the implanted nitrogen atoms are segregated at the interface between the substrate and the sidewall SiO_2 by a low temperature heat treatment. This forms a silicon nitride layer under the sidewall SiO_2 which can suppress the hot electron injection.

However, this technique limits the nitrogen atom segregation to the area under the SiO_2 sidewall. Due to the high electric field strength, the structure cannot suppress

the hot carrier injection into the gate oxide, since the nitrogen segregated area only covers the region under the CVD deposited SiO_2 sidewall spacer.

Hence, there is a need for processing techniques that are more suited for preventing punchthrough and hot carrier degradation of CMOS FETs in ULSI applications. There is a particular need for processing techniques that are capable of preventing hot carrier injection into the gate of the transistor.

Summary of the Invention

The aforementioned needs are satisfied by the process of the present invention which comprises a process to improve hot carrier resistance of a transistor gate by isolating the gate polysilicon with a nitride film. A typical transistor structure is a channel region defined by a source and a drain region formed in a semiconductor wafer. A gate structure is then positioned on the wafer above the channel region where the gate structure is comprised of an isolating oxide region positioned on the wafer and a polysilicon layer positioned thereon.

In the preferred embodiment, the process of forming an isolating nitride film to isolate gate polysilicon comprises first doping the wafer with a global nitrogen implantation which results in forming nitrogen doped regions in the source and the drain regions of the wafer. Hence, nitrogen doped regions are formed over the wafer. Subsequently, an oxidation process is carried out to oxidize exposed portions of the gate polysilicon and the source and the drain regions. However, under the oxidation conditions two other important phenomenons occur. These are the formation of a polysilicon bird's beak region and the diffusion of nitrogen atoms into the gate region to form silicon nitride. Specifically, during the oxide growth, the oxide layer can also laterally extend under the polysilicon gate edges and form a wedge shaped oxide profile at the poly gate edges. The diffusion of nitrogen atoms from the nitrogen doped regions into these oxidized gate edges also advantageously forms silicon nitride under the gate edges. As is well known, silicon nitride is an excellent dielectric and hence provides an effective protection against current leakage into the gate polysilicon.

These and other objects and advantages of the present invention will become more fully apparent from the following description taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a cross-sectional view of a silicon wafer portion having n-channel and p-channel gate stacks on the top surface;

Figure 2 is a cross-sectional view of the wafer shown in Figure 1 wherein a global nitrogen implantation is applied on the top surface;

Figure 3 is a cross-sectional view of the wafer shown in Figure 2 wherein a layer of silicon dioxide is grown from a gate conductor;

Figure 4 is a cross-sectional view of the wafer shown in Figure 3 wherein P+ and N+ regions are formed and a cap layer is deposited over the partially processed wafer.

Detailed Description of the Preferred Embodiment

As will be described hereinbelow, the preferred embodiment of the present invention is directed to improving hot carrier resistance of CMOS LDD FETs in ULSI applications by implanting nitrogen atoms into the source and drain regions, and subsequently reoxidizing gate polysilicon to segregate nitrogen atoms under the polysilicon edges. Reference will now be made to the drawings wherein like numerals refer to like parts throughout.

Figure 1 shows an exemplary CMOS circuit 100 prepared using conventional process steps up to the point of defining an n-channel MOSFET region 105A and a p-channel MOSFET structure 105B on a silicon substrate 101. Hence, a basic CMOS structure having n-well 102 and p-well 103 regions is formed in the silicon substrate 101. As can be seen in Figure 1, a field oxide region 104 is also formed on the top surface of the substrate 101 at the intersection of the n-well region 102 and the p-well region 103. Further, an n-channel gate stack 106A is formed on the upper surface of the n-well region 102 and a p-channel gate stack 106B is formed on the upper surface of the p-well region 103. Both of the gate stack structures 106A and 106B may, for example, comprise a conductive gate polysilicon 112 deposited over a thin gate silicon oxide 108, an isolating refractory metal silicide or silicon oxide layer 114 deposited on top of the polysilicon 112 layer and finally a silicon nitride upper layer 116 deposited on this refractory layer 114.

LDD regions (not shown in the Figures) can also be formed in the source and drain regions 117 by implanting low/high dose arsenic (for NMOSFETs) and low/high dose phosphorus (for PMOSFETs). After the LDD implantation step, an optional anti-punchthrough halo implantation step of either boron or phosphorus (not shown) may be performed over the source/drain regions 117. It will be appreciated that such LDD formation and halo implantation processes are well known in the art of semiconductor processing and may be integrated in a variety of ways.

Referring now to Figure 2, the in-process CMOS circuitry 100 of Figure 1 is subjected to an ion implantation process with ion dopants selected from a suitable species which can form a preselected silicon-based insulator when reacted with silicon. This ion implantation process forms an ion implanted area 118 in source/drain regions 117 and also in the exposed portions of the substrate 103 (not shown). In the preferred embodiment, the implanted ions are nitrogen ions and the preselected silicon-based insulator is nitride which is formed in the manner explained below. In particular, ion implantation forms a specific concentration and distribution of dopant atoms in the ion implanted areas 118 of the substrate 101. In fact, the implantation process alters the ordered substrate crystal structure and distorts the crystal lattice to accommodate these extra atoms in the implantation area 118.

This type of transformation is called amorphization which is, in this embodiment, caused by nitrogen implant atoms. However, as will be fully understood in the next process step, these amorphous implant areas 118 are advantageously used as a nitrogen atom source during the formation of a nitride insulating layer along the side walls 122 of the gate structures 106A, 106B. Additionally, amorphization of the silicon substrate by implanting nitrogen prevents the out diffusion of LDD implants (As, P, etc.) which reduces the need for the conventional Si or Ge deposition step used to prevent this out diffusion in the prior art.

In the present embodiment, one objective is to provide a dopant nitrogen concentration and distribution that achieves nitrogen atom diffusion into the growing oxide layer. Nitrogen implantation can be accomplished using standard ion implantation. The amount of the nitrogen doping may range from about $1x10^{12}$ atoms

to $1x10^{15}$ atoms. A preferred implantation energy is in the range of about 10 keV to 100 keV.

Referring to Figure 3, following the nitrogen implantation step, a thermal spacer growth step is carried out to form an oxide layer 130 over the source/drain regions 117 and on the sidewall 122 of both n-channel 106A and p-channel 106B transistor gates. This forms a vertical sidewall insulating spacer 126 on the sides of the polysilicon gate 112. This spacer growth step also repairs the implantation damage in the implanted areas 118 and produces a slight bird's beak structure 124 under both the lower edges 127 of each transistor gate poly 112. Due to its shape, this structure 124 is called the "gate bird's beak" or GBB. The GBB 124 increases the thickness of the gate oxide 108 at the lower edges 127 of the gate polysilicon 112 and thereby relieves the electric field intensity at the edges or corners 127 of the gate structure 106. This spacer growth step can be performed using any of the known techniques in the art.

Preferably, the spacer growth comprises a thermal oxidation, such that the spacer 126 comprises oxide. Preferred parameters for the oxidation comprise heating the structure to between about 700°C and 1,100°C, more preferably between about 850°C and 950°C, and most preferably about 907°C. The length of the oxidation may range from about 5 minutes to about an hour, more preferably between about 10 minutes and 20 minutes, and most preferably about 15 minutes. A dry oxygen atmosphere is preferred. Alternatively, the spacer growth may comprise a nitridation step.

This spacer growth step is a heating step, like a conventional post-doping thermal drive step. Unlike prior art drive steps, however, oxidation of the substrate causes upward migration and consumption of silicon atoms from the implanted areas 118 (as well as from the gate poly 112), to form the oxide layer 130. This is accompanied by upward motion of implanted nitrogen atoms. The nitrogen concentration difference between the growing oxide layer 130 and the implanted areas 118 provides the driving force for the reaction. Thus, the implanted nitrogen atoms migrate to the growing oxide layer 130 at the substrate surface and a silicon nitride layer 131 is formed over the implanted source/drain regions 11. As well known in the

art, silicon nitride has a high dielectric constant, higher in particular than silicon oxide, and is an effective barrier or protective layer against hot carrier injection at the gate edges 127, which is otherwise induced by the high electric field present in a ULSI device.

Significantly, the silicon nitride formation 131 also extends laterally at least partially under the gate poly 112 in the region of the GBB 124, due to mobility of atoms during the oxidation, and to form a nitride edge portion at least partially underlying the gate corner 127. The edge portion 133 may form only the oxide/substrate interface, as illustrated, or nitrogen atoms may diffuse through the growing oxide 130 to the gate poly 112. This laterally grown edge portion 133 effectively isolates the lower polysilicon gate edges 127 from the neighboring source/drain regions and thus effectively minimizes the high electric field induced current leakages into the gate poly 112. As previously mentioned, in prior art applications the conventional oxide spacer deposition and the following heat treatment tend to limit the nitride formation to the region under the deposited sidewall spacer. However, this limited prior art isolation fails to adequately protect the device against hot electron injection.

As illustrated in Figure 4, polysilicon sidewall oxidation and silicon nitride formation are preferably followed by a formation of a second spacer 136 around sidewalls of each gate structure, prior to masking steps for N+ implantation in the P-well and P+ implantation in the N-well. The spacers 136 may be conventionally formed by blanket deposition of oxide, for example, followed by anisotropic etch of the horizontal surfaces of the oxide, leaving the vertical sidewall spacers 136 shown in Figure 4.

After the spacers 136 have been formed, conventional source/drain implants may be performed. For the CMOS transistors shown, a masking step protects the N-well while N+ dopants are implanted into the source and drain regions of the P-well. A second masking step protects the P-well while P+ dopants are implanted into the source/drain regions on either side of the gate within the N-well. The spacers 136 serve to protect the channel area underlying the gate from source/drain implants.

Depending upon desired device characteristics, a number of optional doping steps are available to tailor device characteristics. For example, after gate definition, a double-diffuse or "DD" implant of boron may improve short channel characteristics by suppressing punchthrough effect. As an independent option, after forming the source/drain regions through N+/P+ implantation, N+ regions may be doped with a light dose of phosphorus, grading the junction and thereby increasing transistor drive for peripheral NMOSFETs. Similarly, phosphorus-halogen implantation (with the P-wells masked) may improve short channel characteristics of PMOSFETs.

As illustrated in Figure 5, the process may thereafter follow conventional processing steps, including a cap layer 138 of silicon nitride or silicon oxide spacer material, CVD-deposited over the structure to block out diffusion from the BPSG to be deposited. Further conventional steps (not shown) include BPSG deposition, reflow, and contact formation.

It will be understood that the improved transistor gate manufacturing technique provided by the preferred embodiment prevents hot electron injection into the gate polysilicon. As explained, the segregation of implanted nitrogen atoms to the growing oxide layer effectively isolates the gate polysilicon edges and minimizes current leakages into the gate polysilicon. Therefore, the improved performance provided by the present embodiment may enable the present invention to be used in the manufacture of deep sub-half-micron size devices and, in particular, high performance memory arrays.

Hence, although the foregoing description of the preferred embodiment of the present invention has shown, described and pointed out the fundamental features of the invention, it will be understood that various omissions, substitutions, and changes in the detail of the apparatus and method as illustrated as well as the uses thereof, may be made by those skilled in the art, without departing from the spirit of the present invention. Consequently, the scope of the present invention should not be limited to the foregoing discussion, but should be defined by the appended claims.

WHAT IS CLAIMED IS:

1. A process of forming a gate structure on a semiconductor substrate, comprising:

providing a semiconductor substrate having a channel region formed therein so as to define a source and a drain region and a gate structure comprised of a gate dielectric positioned on said channel region and a conductive layer positioned on said gate dielectric;

forming an insulator element region on said substrate; and

transforming a portion of said conductive layer adjacent said insulator element region into a sidewall spacer.

2. The process of Claim 1, wherein forming said insulator element region comprises doping said wafer with said insulator element.

3. The process of Claim 1, wherein said insulator element region comprises said insulator element and silicon.

4. The process of Claim 3, wherein said insulator element comprises nitrogen.

5. The process of Claim 4, wherein forming said insulator element region comprises doping the substrate with greater than about 10^{12} nitrogen atoms.

6. The process of Claim 1, wherein transforming said portion of said conductive layer comprises oxidizing said portion.

7. The process of Claim 6, wherein said conductive layer comprises polysilicon.

8. The process of Claim 6, wherein oxidizing said portion further comprises growing a bird's beak region extending laterally into a selected portion of said conductive layer.

9. The process of Claim 6, where oxidizing said portion further comprises forming a nitride layer on said semiconductor substrate.

10. The process of Claim 9, wherein said nitride layer laterally extends under at least a portion of said conductive layer.

11. The process of Claim 1, wherein said gate dielectric comprises silicon oxide.

12. The process of Claim 1, further comprising depositing a second sidewall spacer over the sidewall spacer.

13. A process of forming a gate structure on a semiconductor wafer comprising the steps of:

providing a semiconductor substrate having a channel region formed therein so as to define a source region and a drain region and a gate structure comprised of an isolation layer positioned on said channel region and a conductive layer positioned on said isolation layer;

implanting an insulator element into said source and drain regions;

oxidizing a portion of said conductive layer adjacent said implanted source and drain regions to form an oxide spacer and a protective layer over said source and drain regions, said protective layer comprising said insulator element and characterized by a dielectric constant higher than that of silicon oxide.

14. The process of Claim 13, wherein oxidizing said portion of said conductive layer comprises growing a bird's beak region extending laterally into a selected portion of said conductive layer and said protective layer extending at least partially under said conductive layer.

15. A process of forming a gate structure on a semiconductor wafer comprising the steps of:

providing a semiconductor wafer having a channel region formed therein so as to define a source and a drain region and a gate structure comprised of an isolation layer positioned over said channel region and a conductive layer positioned over said isolation layer;

implanting nitrogen into said source and drain regions;

transforming a portion of said conductive layer adjacent said insulator element region into an oxide spacer;

combining a portion of said substrate with said nitrogen to form a nitride protective layer over said substrate; and

depositing a sidewall spacer over the oxide spacer.

16. A semiconductor device comprising:

a substrate having a channel region interposed between a source and a drain region;

a gate structure comprised of an isolation layer positioned on said wafer adjacent said channel region and a conductive layer positioned on said isolation layer;

an insulating spacer over a portion of said conductive layer and extending in a gate bird's beak structure; and

a protective film having a higher dielectric constant than silicon oxide extending over said source and drain regions.

17. The semiconductor device in Claim 16, wherein said insulator film comprises an insulator element diffused from an insulator element region formed on said source and drain regions in said substrate.

18. The semiconductor device in Claim 17, wherein said insulator element region is formed by doping said source and drain regions by said insulator element.

19. The semiconductor device in Claim 17, wherein said insulator film is silicon nitride and said insulator element is nitrogen.

20. A semiconductor gate structure comprising:

a silicon channel;

a gate oxide positioned over said silicon channel;

a conductive gate electrode positioned over said gate oxide; and

a silicon nitride film extending at least partially over said silicon channel.

21. The gate structure of Claim 20, wherein the gate structure is a gate in a field effect transistor device.

22. The gate structure of Claim 20, further comprising an oxide spacer on a sidewall of said electrode and extending into a gate bird's beak structure under said electrode.

23. A process of eliminating hot electron injection into a gate electrode positioned on a gate oxide adjacent a channel interposed between a source and a drain region in a silicon substrate, the process comprising:

forming a nitrogen doped region in said source and drain regions; and

forming a silicon nitride film over a portion of said gate electrode so that a portion of said silicon nitride film penetrates under said gate electrode during said forming step wherein said portion of said silicon nitride film prevents hot electron injection into said gate electrode.

24. The process of Claim 23, wherein the step of forming silicon nitride film comprises exposing said gate electrode to an oxidizing ambient.

25. The process of Claim 23, further comprising double diffuse boron implanting said source and drain regions.

26. The process of Claim 23, further comprising:

depositing an insulating layer over said gate electrode; and

anisotropically etching said insulating layer to form sidewall spacers.

27. The process of Claim 24, further comprising source/drain implanting said source and drain regions.

28. The process of Claim 25, further comprising lightly doping said source and drain regions to grade a junction between said channel and said source and drain regions.

FABRICATION OF INTEGRATED DEVICES USING NITROGEN IMPLANTATION

Abstract of the Disclosure

A process is provided for forming an isolating nitride film to isolate gate polysilicon of a gate structure. Specifically, the process comprises providing a channel region defined by a source and drain region of a semiconductor substrate having a gate structure comprising an isolating oxide layer positioned on the channel region and the polysilicon layer positioned on the oxide layer. More specifically, the process comprises the steps of forming the nitrogen implanted regions over the semiconductor substrate by implanting nitrogen atoms into those regions and growing spacers from exposed portions of the polysilicon layer. During the spacer growth, the spacer grows vertically as well as laterally extending under the polysilicon edges. Diffusion of nitrogen atoms to the substrate surface forms silicon nitride under the gate edges, which minimizes current leakages into gate polysilicon.

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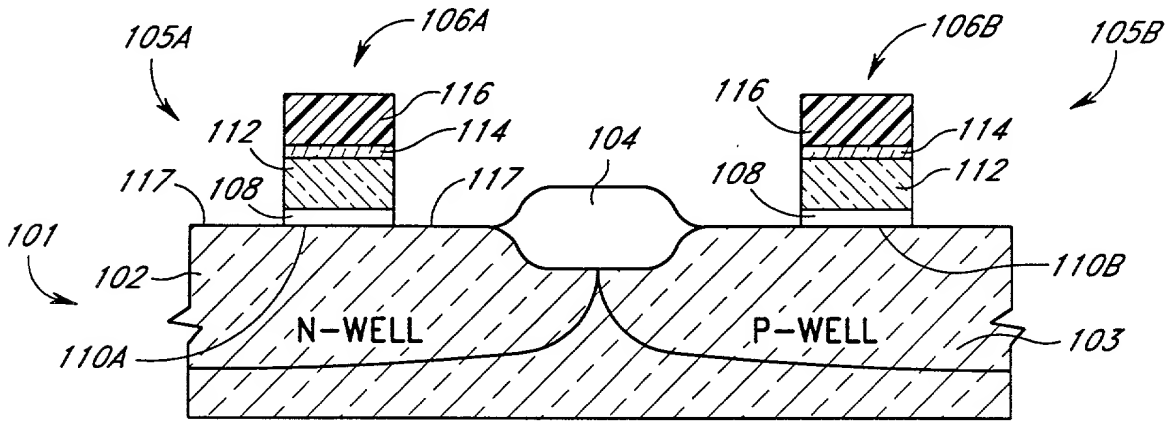
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Fig. 1

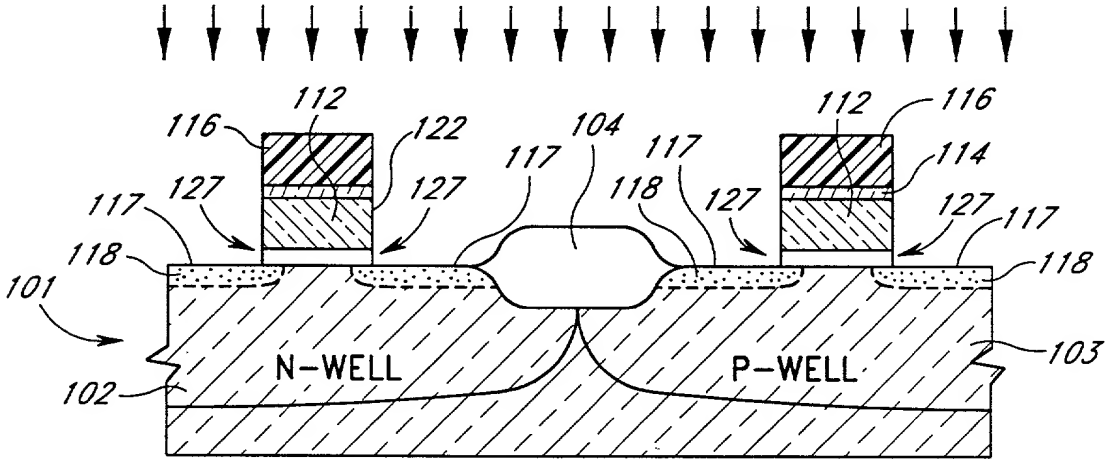
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Fig. 2

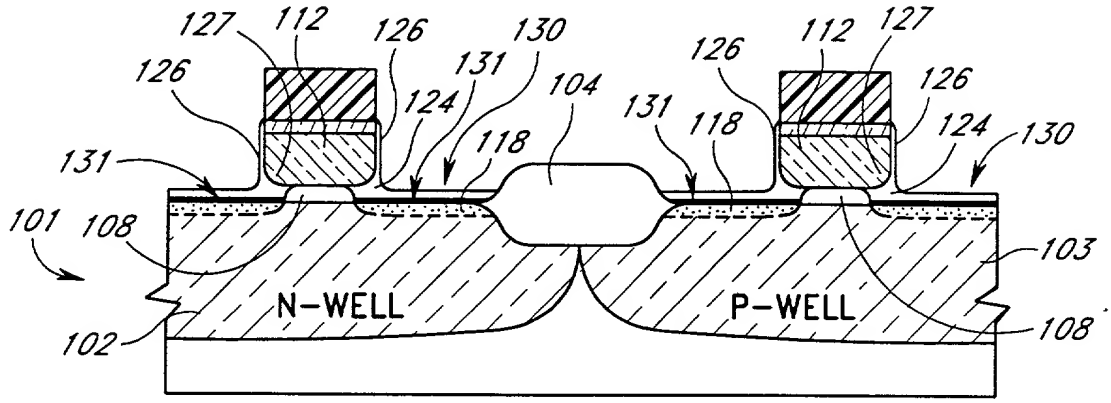

Fig.3

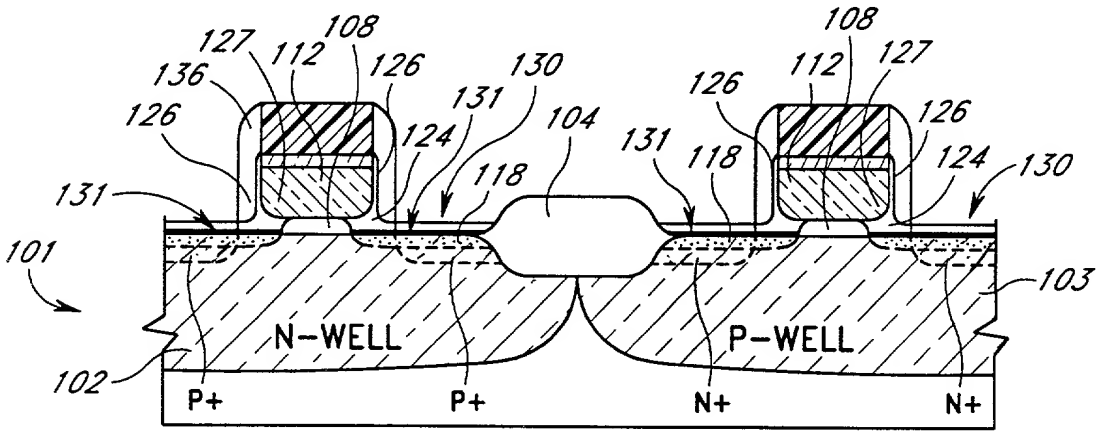

Fig.4

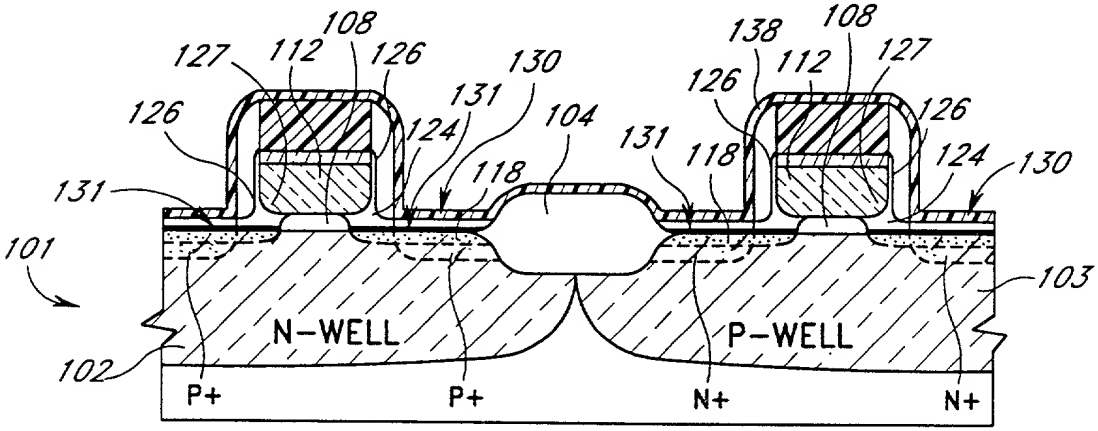

Fig.5

Attorney's Docket No. MICRON.061A

DECLARATION - USA PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled FABRICATION OF INTEGRATED DEVICES USING NITROGEN IMPLANTATION; the specification of which is attached hereto;

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above;

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56;

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole inventor: **Aftab Ahmad**

Inventor's signature _____

Date 6/5/97

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